10-16-00 A

PATENT APPLICATION
Docket No.: 45475-00028
99-44653

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: Sung Sik Jang

For: SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING

CERTIFICATE OF MAILING BY EXPRESS MAIL

"EXPRESS MAIL" Mailing Label No. EL524962024US

Date of Deposit: . . . . . OCTOBER 13, 2000
I hereby certify that the paper(s) and/or fee(s) listed below are attached hereto and are being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents, Washington, D.C. 20231

Type or Print Name: . . . . . Carol A. Woods

. . . . . Carol A Woods
Signature

BOX PATENT APPLICATION
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing, please find the following:

1. (XX) The specification of the above-referenced patent application is enclosed herewith (16 page(s) including claim(s) and Abstract).

2. (XX) 6 sheet(s) of:
X informal drawing(s) is (are) enclosed herewith.
____ formal drawing(s) is (are) enclosed herewith.

3. (X) The fees for this application have been calculated and included as shown below (Prior to calculating the fees, please enter any enclosed preliminary amendment.):

	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				**$710**
TOTAL CLAIMS	**20-20**	**0**	**$18**	**0**
INDEPENDENT CLAIMS	**3- 3**	**0**	**$80**	**0**
MULTIPLE DEPENDENT CLAIM(S) PRESENTED			**$270**	
TOTAL FEES:				**$710.00**
Deduct One-Half for Small Entity Status				
Assignment Recordal Fee			**$40**	
TOTAL AMOUNT DUE:				**$710.00**

4. __ Check(s) in the amount of $_____ is/are enclosed herewith. Please charge any deficiency or credit any overpayment to Deposit Account No. _____.

___ Please charge my Deposit Account No. _____ in the amount of $_____. Please charge any deficiency or credit any overpayment to Deposit Account No. _____.

5. (X) An oath or declaration is enclosed herewith that is:

_X_ Unsigned

____ Newly executed per 37 CFR 1.63(a) and (b).

___ A copy of the executed declaration filed in the prior application upon which priority is based, showing the signature or an indication thereon that it was signed; and:

___ This application is being filed fewer than all of the inventors named in the prior application and it is requested that the following name or names be deleted from the list of inventors in the prior application for this continuation or divisional application:

_____

_____.

___ The prior application was accorded status under 37 CFR § 1.47 and is accompanied by:

___ A copy of the decision granting a petition to accord Sec. 1.47 status to the prior application

(unless all of the inventors have or legal representatives have filed an oath or declaration to join in the prior application).

___ A copy of the subsequently executed oath(s) or declaration(s) filed by the inventor(s) or legal representative(s) that have subsequently joined in the prior application.

6. (X) The power of attorney for this application:

___ is appointed in the newly executed Oath or Declaration submitted herewith.

_X_ is appointed by the power of attorney enclosed herewith.

___ remains the same as originally in the parent application.

___ was changed during the prosecution of the parent application and a copy of the change in the power of attorney is enclosed herewith.

7. (XX) The correspondence address for this application shall be:

Stanley R. Moore, Esq.
Jenkens and Gilchrist, P.C.
3200 Fountain Place
1445 Ross Ave.
Dallas, Texas 75202

_X_ which is a new correspondence address or a change therein.

___ which is the same as originally in the parent application.

___ which is the change in the correspondence address that was filed during the prosecution of the parent application.

8. (XX) Priority is hereby claimed under 35 USC 119 and 172 to the following foreign applications:

Country	Serial No.	Date
Korea	99-44653	Oct. 15, 1999

and:

___ A certified copy of each application is enclosed herewith.

___ A certified copy of each application was filed in prior application Serial No. _____.

9. ( ) A verified statement claiming small entity status under 37 CFR 1.9 and 1.27:

___ is enclosed herewith.

___ was filed in parent application Serial No. _____, and such status remains unchanged and is requested for this application.

10. ( ) A preliminary amendment is enclosed herewith.

11. ( ) An Information Disclosure Statement with Modified PTO Form 1449 and a copy of the cited references are enclosed herewith.

12. ( ) An Assignment of the invention to _____ with cover sheet and recordation fee is enclosed herewith for recordation by the Assignment Branch.

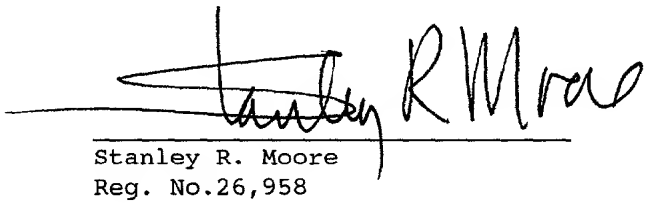
13. ( ) The Commissioner is hereby authorized to charge payment, or to credit any overpayment, of the following fees associated with this filing or during the pendency of this application to Deposit Account No. _____.

___ Any patent application filing fees under 37 CFR 1.16.
___ Any patent application processing fees under 37 CFR 1.17.
___ The issue fee under 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).

14. ( ) Other (specify):_____
_____
_____.

15. (XX) Confirmation Postcard.

Respectfully submitted,



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Patent Application
Docket #45475-00028
99-44653

SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING

TECHNICAL FIELD

The present invention relates in general to a semiconductor package, and more particularly but not by way of limitation, to a semiconductor package in which the adhesiveness between a chip paddle and a package body is improved, and the chip paddle ground-bonding is improved.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski and incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of

electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, consumer demand increases. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

However, this conventional semiconductor package is problematic in that a thickness of the silver plated layer formed on the upper faces of the chip paddle and the internal leads deteriorate the adhesiveness between the package body and the chip paddle or the internal leads. That is, the silver-plated layer is very weakly bonded to the package body of the encapsulation material (the chip paddle or the side of the internal lead, both of which are made of copper, are strongly bonded to the package body), so that interfacial exfoliation is easily caused at the boundary between the package body and the silver-plated layer. Further, moisture can readily permeate the semiconductor package through the exfoliated portion, which may cause the semiconductor package to crack.

Usually a semiconductor chip or a chip paddle is ground-bonded by conductive wires to achieve grounding or eliminate electrical noise problems. In this conventional semiconductor package, the semiconductor chip is similar in area to the chip paddle, so that there are no sufficient areas for ground bonding.

SUMMARY OF THE INVENTION

In one embodiment of the present invention, there is provided a semiconductor chip having an upper surface and a bottom surface. A plurality of input bond pads and output bond pads on the upper surface of the semiconductor chip and along the circumference of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle is provided which has a top surface, a side surface and a bottom surface. The chip paddle is bonded to the bottom surface of the semiconductor chip by an adhesive. The chip paddle has corners, a circumference and a half-etched section at the lower edge of the chip paddle along the chip paddle circumference.

A leadframe is provided having a plurality of tie bars. Each of the tie bars has a side surface and a bottom surface. The plurality of tie bars are connected to the corners of the chip paddle. The plurality of the tie bars externally extend from the chip paddle and have a half-etched section. A plurality of dam bars are provided on the leadframe help limit flow of encapsulation material on the leadframe.

A plurality of internal leads connect to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the circumference to the chip paddle and extend towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle.

A ground ring is provided having an upper surface and a lower surface, and positioned between the semiconductor chip and the plurality of internal leads. The ground ring may interchangeably be used as a ground or a power ring. The upper surface of the ground ring is substantial planar with the upper surface of the semiconductor chip and the upper surface of the plurality of internal leads. A plurality of conductive wires are electrically connected to the plurality of internal leads and the semiconductor chip, wherein the conductive wires have a loop height between the leads and the semiconductor chip. Because of the planarity of the grounding leads and semi-conductor chip, the loop height of the conductive wires is minimized, which allows smaller packaging.

Encapsulating material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. After encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective side and bottom surfaces. The chip paddle further has through-holes in the half-etched section of the chip

paddle for increasing the bonding strength of the encapsulation material in the package body. In addition, tabs in the half-etched section of the chip paddle may be provided for the same purpose.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying Drawings wherein:

FIGURE 1 is a top plan view of the semiconductor chip of the present invention;

FIGURE 2 is a side elevation cross-section view of the semiconductor chip of FIGURE 1 taken along line 2-2;

FIGURE 3 is a side elevation cross-section view of the semiconductor chip of FIGURE 1 taken along line 3-3;

FIGURE 4 is a top plan view of a leadframe for the semiconductor package of the present invention;

FIGURE 5 is a top plan view of an alternate embodiment for the semiconductor package of the present invention; and

FIGURE 6 is a side elevation cross-section view of the semiconductor package of FIGURE 5 taken along line 6-6.

DETAILED DESCRIPTION

Referring first to FIGS. 1 through 3, a semiconductor package 10 is shown construed in accordance with the principals of the present invention. A semiconductor package 10 includes a semiconductor chip 20 having an upper surface 30, a circumference 40 and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70 are disposed on the upper surface 30 of the semiconductor chip 20. A chip paddle 80 having a top surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a circumference 140 and a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

Referring now to FIGS. 1 through 4 in combination, a leadframe 170 is shown having a plurality of tie bars 180, a side surface 190 and a bottom surface 200. The tie bars 180 are connected to the corners 130 of the chip paddle 80. The tie bars 180 externally extend from the chip paddle 80. The leadframe 170 further has a half-etched section 210 and a plurality of dam bars 220.

A plurality of leads 230 are connected to the leadframe 170 and have an upper surface 235 and a bottom surface 250. The leads 230 are radially formed at regular intervals along the circumference 140 and spaced apart from the circumference 140 of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260 facing the chip paddle 80. It is to be noted that the hatched areas in FIG. 1 are the half-etched sections of the paddle 80 and leads 230.

Referring to FIG. 2, there is disclosed a ground ring 262 formed in the half-etched section 150 of the chip paddle 80. The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230. The ground ring may be interchangeably used as a power ring should circumstances require. The upper surface 264 of the ground ring 262 is planar with the upper surface of the semiconductor chip 20 and the upper surface 235 of the leads 230.

A plurality of conductor wires 270 are provided and electrically connected to the plurality of leads 230 and the semiconductor chip 20. The plurality of conductive wires 270 have a loop height 275 between the plurality of leads 230 and the semiconductor chip 20. The loop height 275 of the conductive wires 270 is minimized from the upper surface 235 of the leads 230 and the upper surface 30 of the semiconductor chip 20. To form the semiconductor package 10, encapsulation material 280 encapsulates the semiconductor chip 20, conductive wires 270, chip paddle 80, and leads 230. Encapsulation material 280 may be thermoplastics or thermoset resins, with thermoset resins including silicones, phenolics, and epoxies. The dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170. During encapsulation, the chip paddle 80, leads 230, and tie bars 180 are externally exposed at the respective side and bottom surfaces. The side and/or bottom surfaces or chip paddle 80, leads 230, and tie bars 180 may be, but do not necessarily have to be, electroplated with corrosion-minimizing materials such as tin lead, tin, gold, nickel palladium, tin bismuth, or similar alloys. In a first embodiment, the chip paddle 80 is provided with a plurality of through holes 300 in the half-etched section 150 for increasing the bonding strength of the encapsulation material 280 with the package 10.

The through holes 300 may be formed by chemical etching, such as when patterning the entire leadframe 170 for forming the half-etched section 150 of the chip paddle 80. Alternatively, the through holes 300 may be formed by the use of a

mechanical punch or similar device. It should be noted that other methods may be used to form the through holes 300, and the present invention is not limited by the formation techniques disclosed herein.

Referring now to FIGS. 4 and 5 in combination, an alternate embodiment for the semiconductor package 10 is shown. In this embodiment, the chip paddle 80 is provided with a plurality of tabs 310 in the half-etched section 150 of the chip paddle 80 for the similar purpose of increased bonding strength. It is also contemplated that the combination of through holes 300 and tabs 310 may be used to increase the bonding strength of the encapsulation material 280 in the package 10.

The tabs 310 are formed in the half-etched section 150 of the chip paddle 80. The tabs 310 must extended to a limited degree to prevent a short circuit forming between the tabs 310 and the leads 230. It is preferable that the number of the tabs 310 corresponds to the number of the grounding input bond pads 60 and output bond pads 70 of the semiconductor chip 20. The tabs 310 may be formed by chemical etching when patterning the entire leadframe 170 and also by other mechanical methods depending on the requirements of the individual package 10. By increasing the area or length of the chip paddle 80, the tabs 310 are easily bonded with conductive wires 270 by increasing the area for which to connect the conductive wires 270. The tabs 310 may serve to function as a ground or power ring 262 in certain applications. It is to be noted that the hatched areas in FIG. 5 are the half-etched sections of the paddle 80 and leads 230.

As described previously, the use of the through holes 300 and tabs 310 increase the bonding strength to the encapsulation material 280, in addition to improving the fluidity of the encapsulation material 280 upon encapsulating. The presence of the through holes 300 and tabs 310 improves the fluidity of encapsulation material 280 by directing flow over or through the tabs 310 and through holes 300 in the package 10. In certain embodiments, as shown in FIGS. 2 and 3, a plated layer 320 of a material such as gold or silver may be applied to the upper surfaces 90, 235 of the chip paddle 80 and leads 230, respectively, to increase bonding strength to the wires 270.

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. While the semiconductor package having improved adhesiveness and crown bonding shown as described as being preferred, it will be obvious to a person of ordinary skill in

the art to add various changes and modifications may be made therein without departing from the spirit and the scope of the invention.

The previous description is of a preferred embodiment for implementing the invention, and the scope of the invention should not necessarily be limited by this description. The scope of the present invention is instead defined by the following claims.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

5

Attorney Docket No.	Title of Application	First Named Inventor
45475-00015	Semiconductor Package Having Increased Solder Joint Strength	Kil Chin Lee
45475-00016	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
45475-00018	Near Chip Size Semiconductor Package	Sean Timothy Crowley
45475-00019	Semiconductor Package	Sean Timothy Crowley
45475-00020	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
45475-00021	Stackable Semiconductor Package and Method for Manufacturing Same	Jun Young Yang
45475-00024	Method of and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
45475-00029	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung

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It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.

What is claimed is:

1. A packaged semiconductor, comprising:

a semiconductor chip having an upper surface, a circumference and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said circumference electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

2. The packaged semiconductor of claim 1, wherein said chip paddle has a circumference and said half-etched section is located at a lower edge of said chip paddle along said chip paddle circumference.

3. The packaged semiconductor of claim 1, wherein said plurality of tie bars each has a side surface and a bottom surface.

4. The packaged semiconductor of claim 1 each of said plurality of tie bars externally extend has a half-etched section.

5. The packaged semiconductor of claim 1, further comprising a ground ring, said ground ring

being electrically connected to said semiconductor chip by said conductive wires.

6. The packaged semiconductor of claim 1, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

7. The packaged semiconductor of claim 1, wherein said chip paddle has a plurality of tabs in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

8. A packaged semiconductor, comprising:

a semiconductor chip having an upper surface, a circumference and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said circumference electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip

by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of tabs in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

9. The packaged semiconductor of claim 8, wherein said chip paddle has a circumference and said half-etched section is located at a lower edge of said chip paddle along said chip paddle circumference.

10. The packaged semiconductor of claim 8, wherein said plurality of tie bars each has a side surface and a bottom surface.

11. The packaged semiconductor of claim 8 each of said plurality of tie bars externally extend has a half-etched section.

12. The packaged semiconductor of claim 8, further comprising a ground ring, said ground ring

being electrically connected to said semiconductor chip by said conductive wires.

13. The packaged semiconductor of claim 8, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

14. The packaged semiconductor of claim 8, wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

15. A packaged semiconductor, comprising:

a semiconductor chip having an upper surface, a circumference and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said circumference electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body; and

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

16. The packaged semiconductor of claim 15, wherein said chip paddle has a circumference and said half-etched section is located at a lower edge of said chip paddle along said chip paddle circumference.

17. The packaged semiconductor of claim 15, wherein said plurality of tie bars each has a side surface and a bottom surface.

18. The packaged semiconductor of claim 15 each of said plurality of tie bars externally extend has a half-etched section.

19. The packaged semiconductor of claim 15, further comprising a ground ring, said ground ring

being electrically connected to said semiconductor chip by said conductive wires.

20. The packaged semiconductor of claim 15, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

ABSTRACT OF THE INVENTION

A semiconductor package having improved adhesiveness between the chip paddle and the package body and having improved ground-bonding of the chip paddle. A plurality of through-holes are formed in the chip paddle for increasing the bonding strength of encapsulation material in the package body. A plurality of tabs are formed in the chip paddle may also be used alone or in conjunction with the through-holes to further increase the bonding strength of the encapsulation material in the package body. The tabs provide additional area for the bonding site to ground wires from the semiconductor chip by increasing the length of the chip paddle.

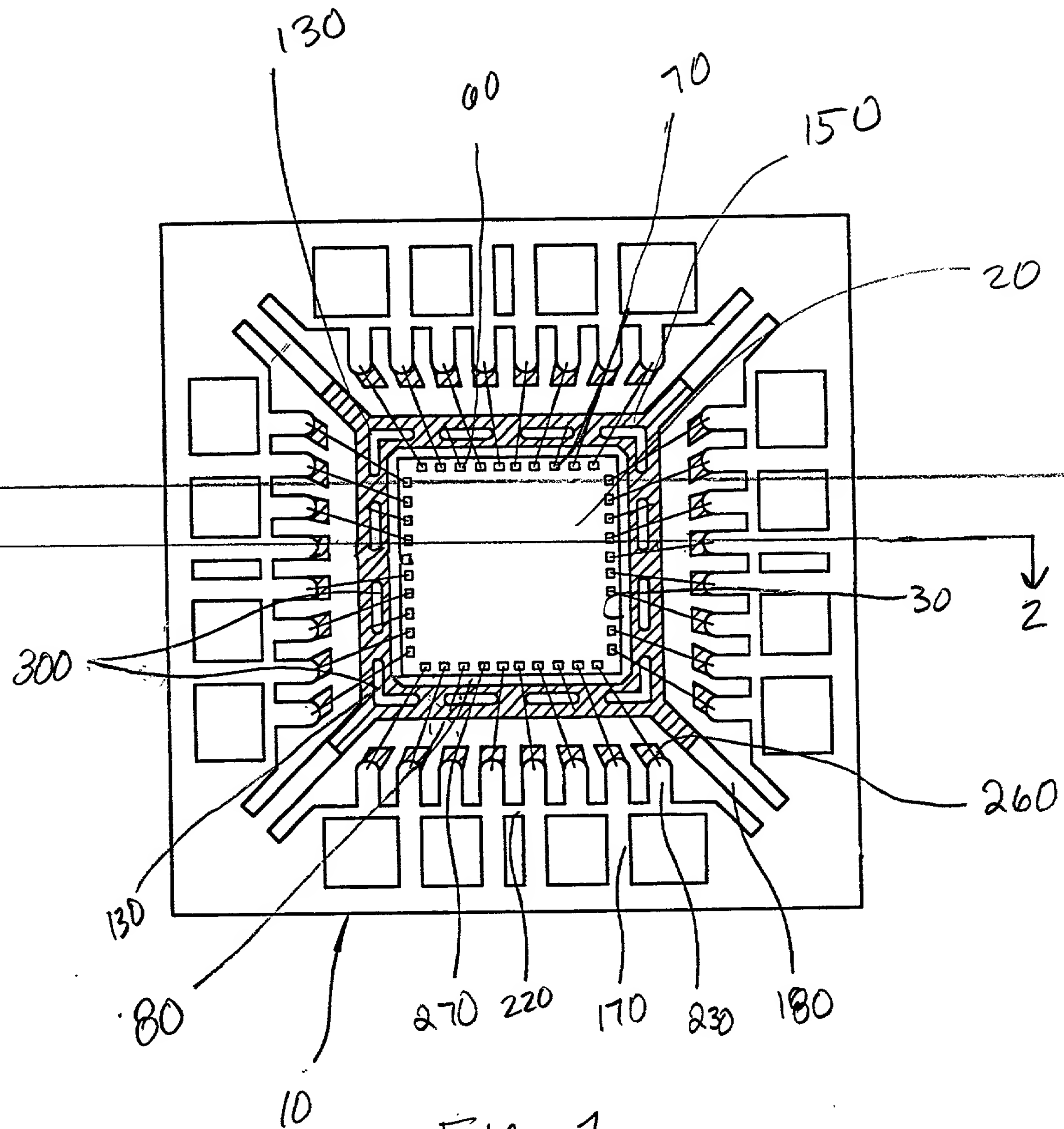

FIG. 1

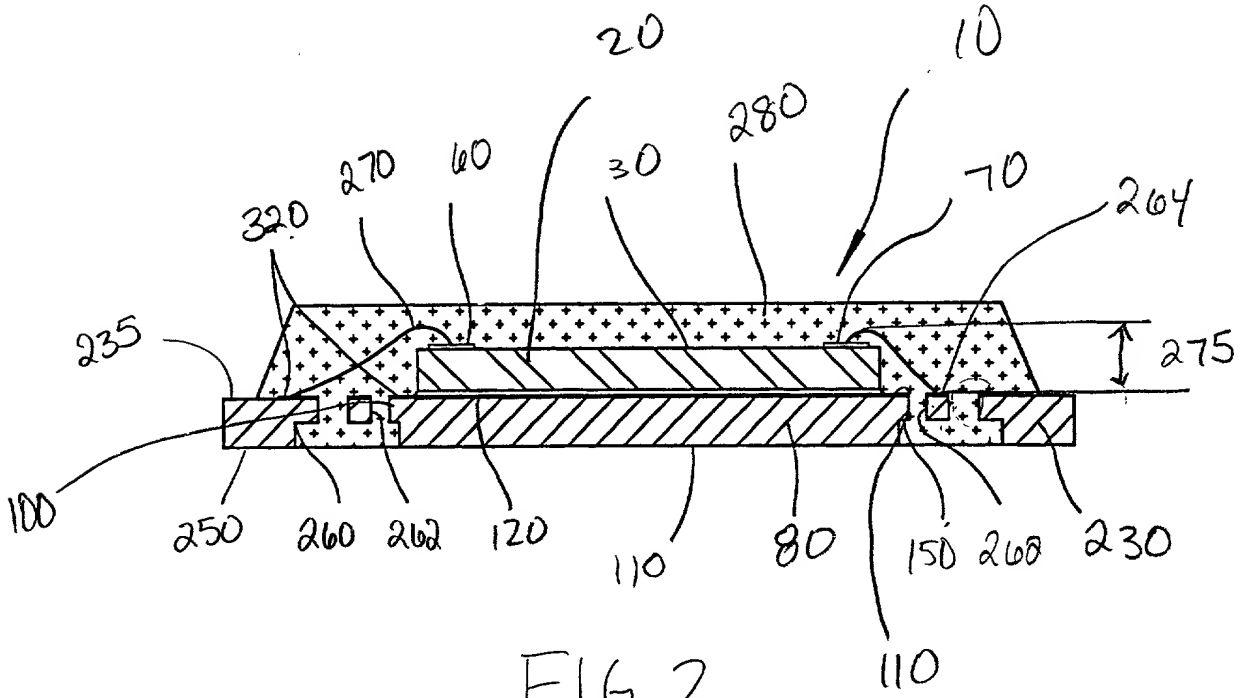
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FIG. 2

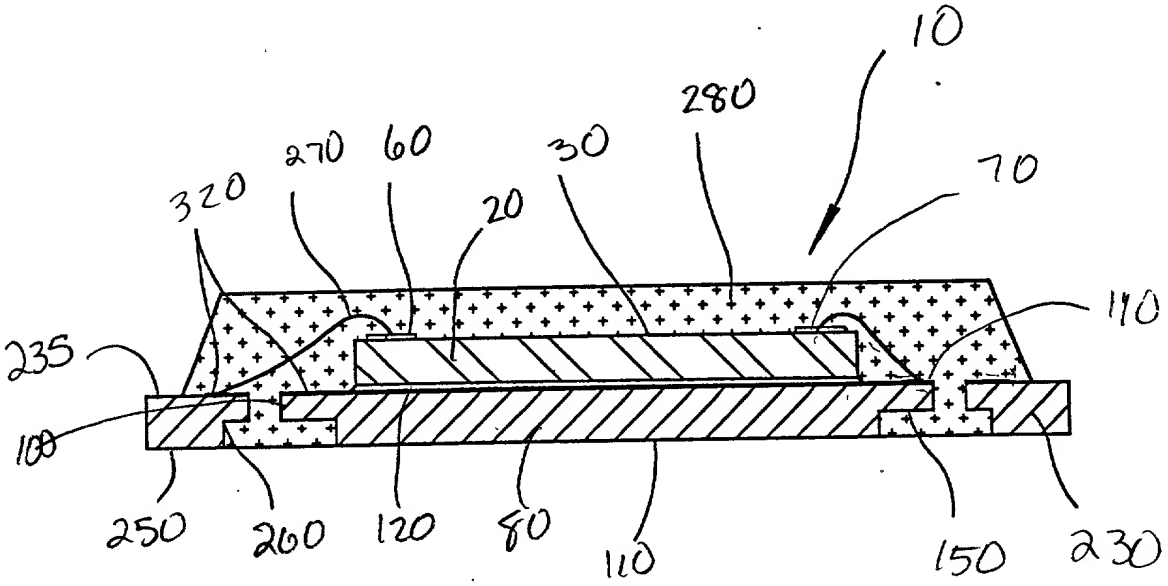

FIG. 3

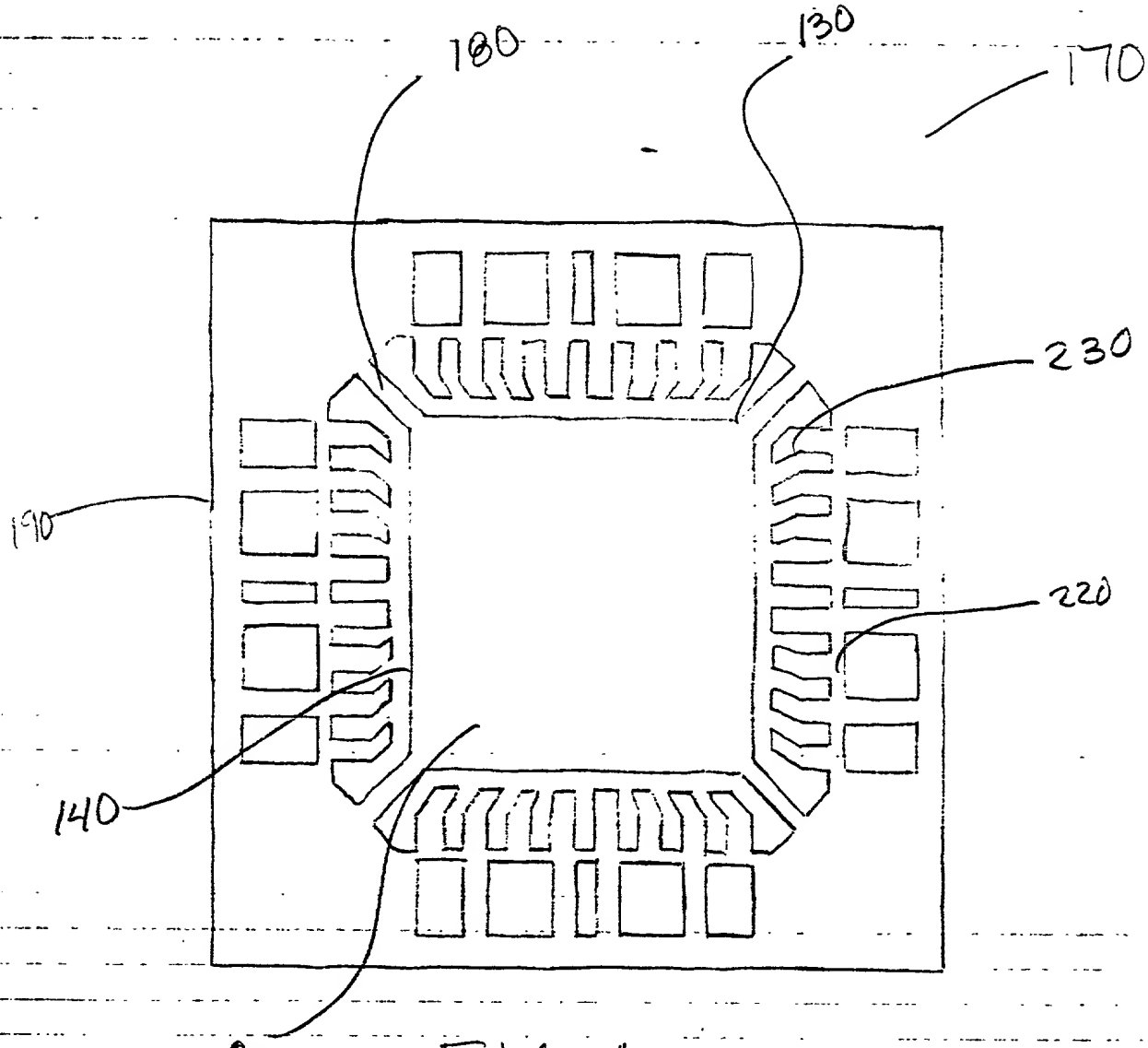

FIG. 4

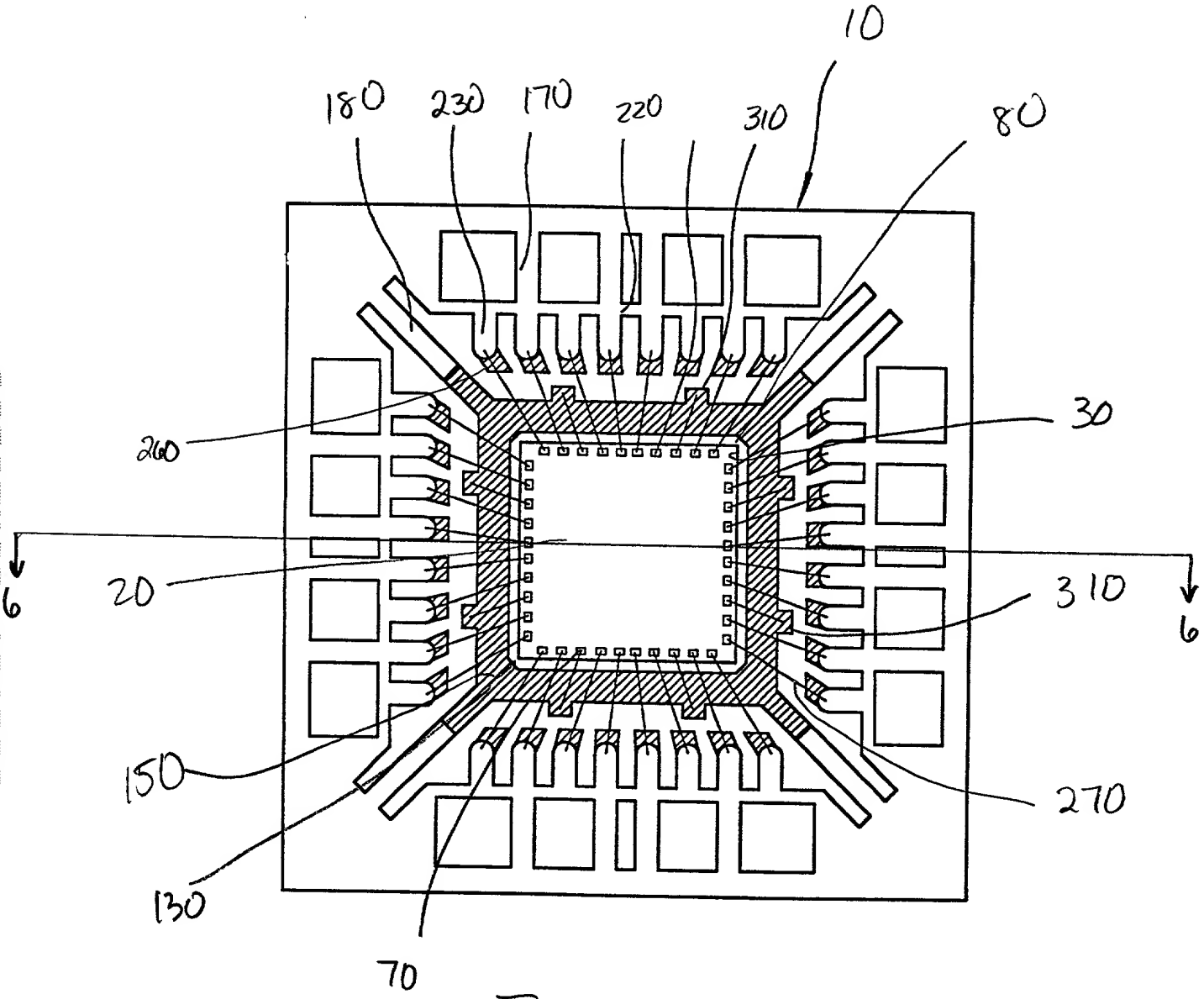

FIG. 5

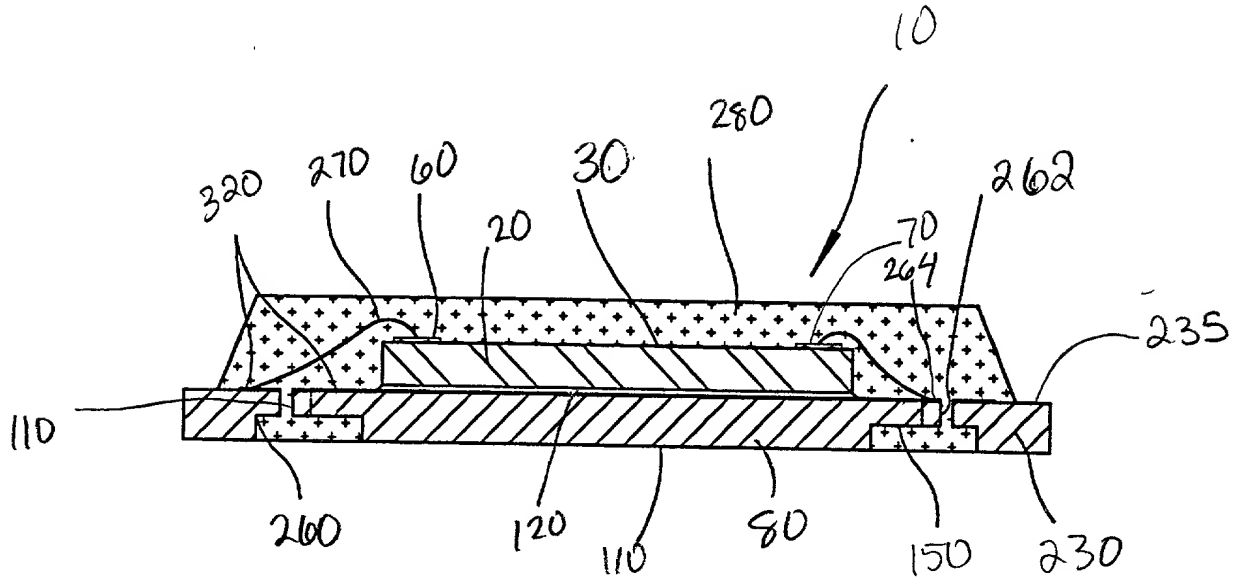

FIG. 6

PATENT APPLICATION
DOCKET NO.: 45475-00028
99-44653

RULES 63 AND 67 (37 C.F.R. 1.63 and 1.67)
DECLARATION AND POWER OF ATTORNEY

FOR UTILITY/DESIGN/CIP/PCT NATIONAL APPLICATIONS

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING,** the specification of which: (mark only one)

X	(a)	is attached hereto.
___	(b)	was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)
___	(c)	was filed as PCT International Application No. PCT/_____ on ____ and was amended on _____ (if applicable).
___	(d)	was filed on ___ as Application Serial No. ___ and was issued a Notice of Allowance on ____.
___	(e)	was filed on _____ and bearing attorney docket number _____ .

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this application as defined in 37 CFR § 1.56. If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application

on which my priority is claimed or, (2) if no priority is claimed, before the filing date of this application:

PRIOR FOREIGN PATENTS

Number	Country	Month/Day/Year Filed	Date first laid-open or Published	Date patented or Granted	Priority Claimed Yes	No
99-44653	Korea	Oct. 15, 1999			XX	

I hereby claim the benefit under 35 U.S.C. § 120/365 of any United States application(s) listed below and PCT international applications listed above or below:

PRIOR U.S. OR PCT APPLICATIONS

Application No. (series code/serial no.)	Month/Day/Year Filed	Status(pending, abandoned, patented)

NONE

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